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Analysing of Software Tools for Designing and Simulating of Digital Circuits

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Abstract: *This paper describes the results of individual and comparative analysis of three software tools for designing and simulating of digital circuits: Cedar Logic Simulator, Deeds-DcS – Digital Circuit Simulator and Proteus 8 Demonstration. As a result, we obtained certain conclusions that could help students of Electrical, Computer and Mechatronics Engineering undergraduate study programs at the Faculty of Technical Sciences Čačak, University of Kragujevac and also students from other Universities to choose the appropriate software tool for designing and simulating digital circuits. For the purpose of individual analysis of these simulators, we designed an example of digital circuit that includes two 4-bit PIPO (Parallel Input Parallel Output) registers, ALU (Arithmetic Logic Unit) and 7-segment display by each tool. The results of analysis showed that the best performance has Deeds-DcS – Digital Circuit Simulator, then Proteus 8 Demonstration and finally Cedar Logic Simulator.*

Keywords: *designing; simulating; digital circuits; analysis of simulators; CEDAR Logic Simulator*; Deeds-DcS – Digital Circuit*; Proteus 8 Demonstration*

1. INTRODUCTION

Designing, simulating and testing of digital circuits using simulation software tools is very important for students who listen to subjects such as Fundamentals of Computer Science, Digital electronics [1] and etc. Economic pressures on universities and the emergence of new technologies have spurred the creation of new systems for delivering engineering laboratories in education, in particular simulations and remote-access laboratory systems [2]. When students completed virtual labs and were then given a face-to-face practical, they performed better than those students who completed the same lab in a traditional (face-to-face) manner [3].. Therefore using these software simulators, students will gain more practical knowledge and experience of theory. The usage of different simulators can lead us to the conclusion which is the best simulator for students' education. Different software tools are used for designing and simulating of digital circuits. Some of the most common are Logisim [4], Xilinx ISE Design Suite [5], LogicWorks [6], LOGiX [7], Digital-ProfiLab [8] and many others. Measurement the advantages of using Logisim in achieving course learning objectives and outcomes as well as student satisfaction with this innovative teaching method was presented in [9]. Results confirmed that students are interested in using this software tool because of its simplicity of use, effectiveness, free availability, system independency, and its ability to check and to simulate the functionality of the designed circuit using only a hand tool. Easy usability is an important consideration especially for first-year students. Students should focus on learning contents of the courses and not to master the features of a tool [10].

In this paper, we analyzed the following tools for designing and simulation of digital circuits: Cedar Logic Simulator [11], Deeds DcS - Digital Circuit Simulator [12] and Proteus 8 Demonstration [13]. The main goal of this paper is to test these three software tools in order to determine which of these tools is the best for targeted user group (in this case students of technical faculties).

The example of digital circuit used in this paper has two 4-bit PIPO (Parallel Input Parallel Output) registers named A and B that have possibility of self-incrementing and self-decrementing. Outputs of registers are inputs of 4-bit ALU (Arithmetic Logic Unit), which was designed by 4-bit Full Adders. Outputs of ALU is 7-segment display and also C, N, Z and V indicators. Realization of this digital circuit trough mentioned simulators is excellent for student's understanding of practical application of

designing digital circuit's theory but also for tracking results of tested simulation. These understandings are very important for any future engineer.

2. DESCRIPTION OF DIGITAL CIRCUIT EXAMPLE

As we already mentioned the example of digital circuit consists of two 4-bit PIPO registers named A and B, where each of them has possibility of self-incrementing and self-decrementing. Registers A and B are implemented using 4 JK flip flops, where *i-th* inputs J_i and K_i are defined by equation (1). Signal *NOP* is defined by equation (2) and it has active value when all control signals are not active. When *NOP* signal is activated, value of state of *i-th* register Q_i will not change because $J_i = K_i = 0$ [14]. For parallel reading, the output of *i-th* register Q_i is multiplied by control signal *RD* (READ). Figure 1 presents *i-th* bit level of register A (it is the same for register B but for this register, A tags should be replaced with B tags).

ALU is designed by Full Adders and it is capable of providing 8 different binary operations (Table 1). [15]. Three control select inputs are named S_1, S_0 and C_{in}. In Table 1 Y_i is *i-th* bit of *B* input and is defined by equation (3). Indicators *C*, *N*, *Z* and *V* that describe the result of ALU's operations are defined by equation (4) [14]. Figure 2 presents *i-th* bit level of Full Adder that is used for designing of ALU.

$$\begin{aligned} J_i &= NOP \cdot 0 + LDI_i + INC \cdot C_i + DEC \cdot \mathrm{E}_i \\ K_i &= NOP \cdot 0 + LD\overline{I_i} + INC \cdot C_i + DEC \cdot \mathrm{E}_i \end{aligned} \quad (1)$$

$$\mathrm{NOP} = \overline{(\mathrm{LD} + \mathrm{INC} + \mathrm{DEC})} \quad (2)$$

Table 1. *Specification for ALU* [15]

S_1	S_0	C_{in}	Y_i	F
0	0	0	0	$F = A$
0	0	1	0	$F = A + 1$
0	1	0	*B*i	$F = A + B$
0	1	1	*B*i	$F = A + B + 1$
1	0	0	$\bar{B}$i	$F = A + \bar{B}$
1	0	1	$\bar{B}$i	$F = A + \bar{B} + 1$
1	1	0	1	$F = A - 1$
1	1	1	1	$F = A$

$$Y_i = S_0 B_i + S_1 \overline{B_i} \quad (3)$$

$$\begin{aligned} C &= C_4 \\ N &= F_3 \\ Z &= \overline{F_0 + F_1 + F_2 + F_3} \\ VADD &= A_3\, B_3 \overline{F_3} + \overline{A_3}\,\overline{B_3} F_3 \\ VSUB &= \overline{A_3} B_3 F_3 + A_3 \overline{B_3}\,\overline{F_3} \end{aligned} \quad (4)$$

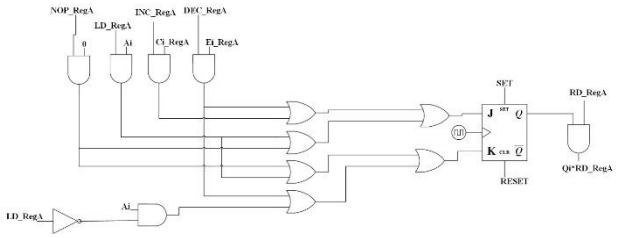

Figure 1. *I-th bit level of A register*

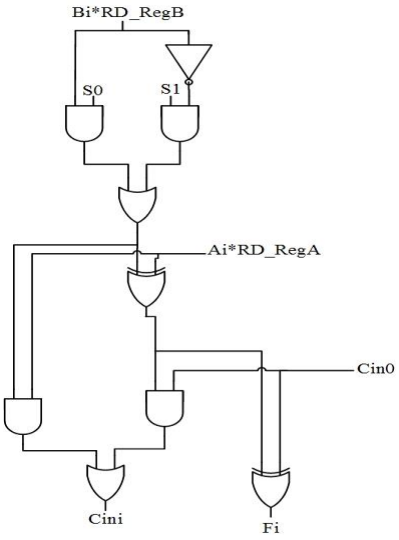

Figure 2. *I-th bit level of Full Adder*

3. CEDAR LOGIC SIMULATOR

Figure 3 presents starting window of CEDAR Logic Simulator. From figure 3 on starting window you can see:

1. Menu Bar – includes different options for saving and editing file, view settings, help and etc.;
2. Available libraries – includes different operations and settings for designing and simulating of digital circuits;
3. Toolbar – includes the most important settings from Menu Bar but also includes options for starting and stopping of simulation and also settings for managing value of Clock half period;
4. Pages – enable splitting of scheme to more than one page (page 1-10);
5. Working area – The area in which users design digital circuits;
6. Available logic elements – graphic interpretation of logic elements with multiple inputs. The usage of logic elements for designing digital circuits is done by ''drag and drop'' mechanism at working area.

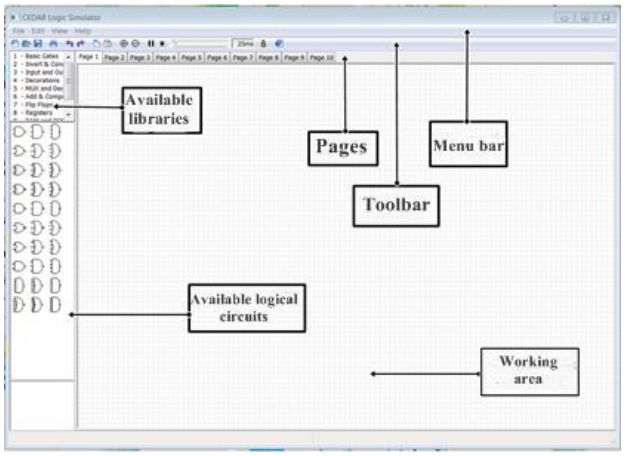

Figure 3. *Starting window of CEDAR Logic Simulator*

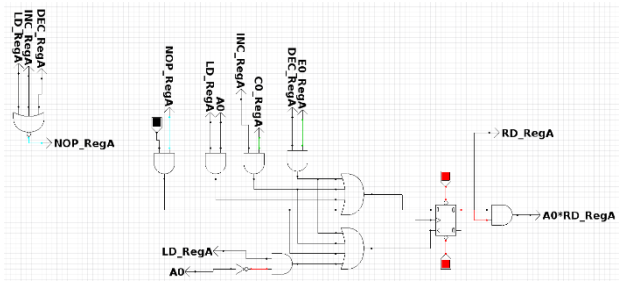

Figure 4. *Zero-bit level of register A realized in Cedar Logic Simulator*

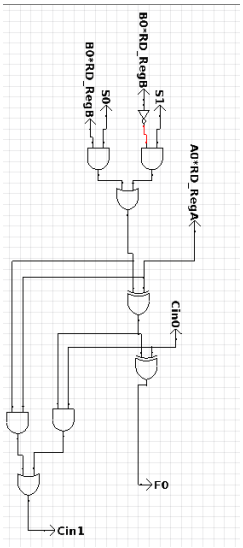

Figure 5. *Zero-bit level of Full Adder realized in Cedar Logic Simulator*

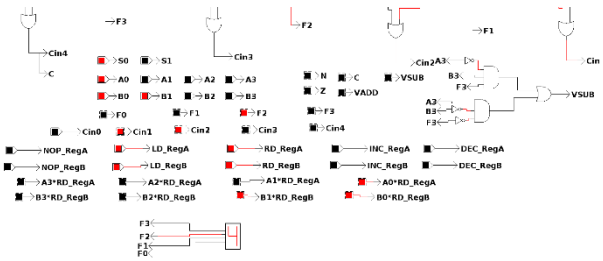

Figure 6. *Result of operation when $S_1S_0C_{in}$=010, A=0001 and B=0011 in Cedar Logic Simulator*

4. DEEDS-DcS – Digital Circuit Simulator

Figure 7 presents starting window of Deeds-DcS - Digital Circuit Simulator. From figure 7 on starting window you can see:

1. Menu Bar - includes different options for saving and editing file, view settings, simulation settings, additional tools, help and etc.;
2. Toolbars – First toolbar includes the most important options from Menu bar but also includes options for Error Check, starting simulation and option for choosing Deeds-FsM Simulator (Finite State Machine Simulator) or Deeds–Mce Simulator (Micro Computer Emulator) that are included in Deeds software package. The main features provided by the Deeds-FsM and Deeds-McE are finite state machine editor/simulator, embedded micro-computer emulator, assembler/interactive debugger module, VHDL converter and FPGA module. This toolbar also includes tools that are used for designing and simulating of digital circuits. Second toolbar includes graphics icons that enable different options (included in drop menus) which are needed for designing and simulating of digital circuits;
3. Working area – The area in which users design digital circuits;
4. Status Bar – Shows description when user's cursor crosses over some icon.

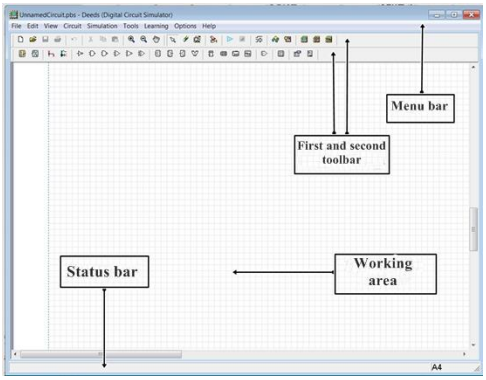

Figure 7. *Starting window of Deeds-DcS – Digital Circuit Simulator*

Figure 8 presents *i-th* bit level of register, while Figure 9 presents *i-th* bit level of Full Adder used to design scheme described in Chapter 2. In Figure 8 and 9 are presented schemes for block elements (build components that can be reused in another circuit). Figure 10 presents realized scheme for following block elements: *VADD*, *VSUB*, *Z* indicators and *NOP* signal.

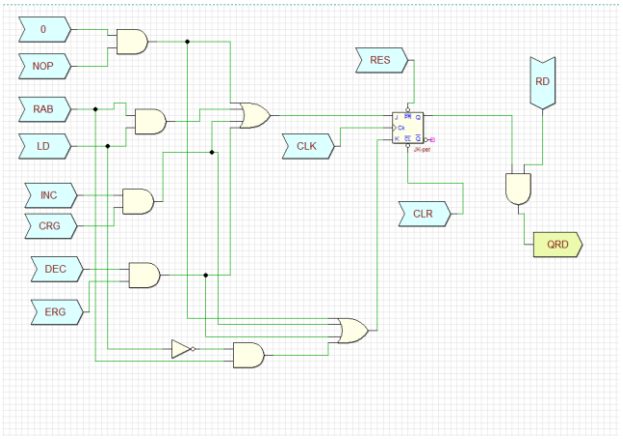

Figure 8. *I-th bit level of register realized for block element in Deeds-DcS - Digital Circuit Simulator*

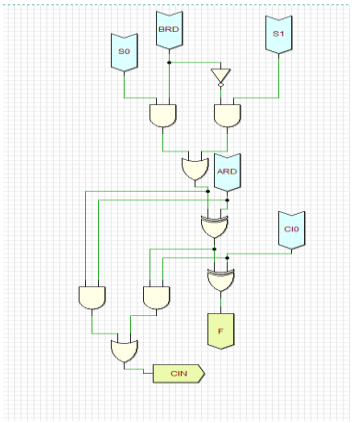

Figure 9. *I-th bit level of Full Adder realized for block element in Deeds-DcS - Digital Circuit Simulator*

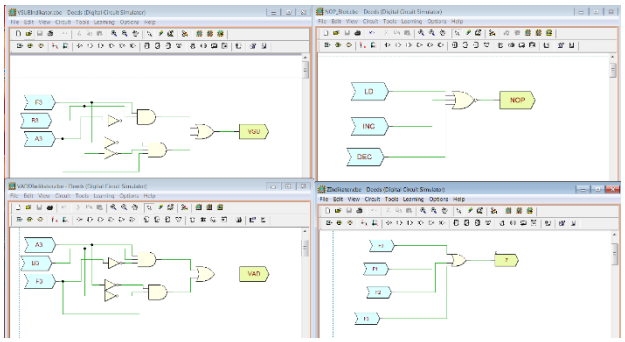

Figure 10. *VADD, VSUB, Z indicators and NOP signal realized for block element in Deeds-DcS - Digital Circuit Simulator-u*

Example of digital circuit, described in Chapter 2 is realized by block elements. Figure 11 presents one part of the realized schema, after the animation for the following control and input signals: $S_1S_0C_{in}$=*010, A=0001 and B=0011* is started.

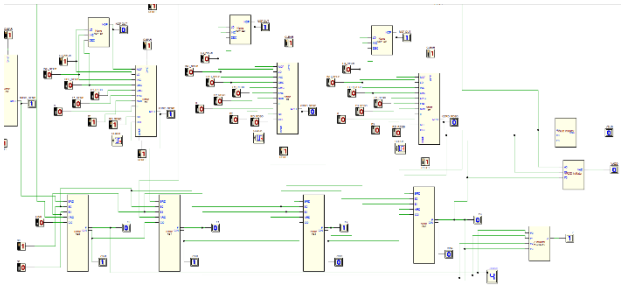

Figure 11. *One part of realized schema and started animation in Deeds-DcS - Digital Circuit Simulator-u*

5. PROTEUS 8 DEMONSTRATION

Figure 12 presents Starting window of Proteus 8 Demonstration. From figure 12 you can see:

1. Menu Bar and Toolbars – includes different options for saving and editing file, view settings, help and etc.;
2. Overview Window – enables overview of schema from bird's perspective;
3. Object selector – presents list of selected objects (components) which a user can choose for designing of schema;
4. Editing area – The area in which a user designs schema;
5. Vertical Tool Mode Toolbar – includes the most important options for designing and simulating of digital (and other) circuits.

Figure 13 presents zero-bit level of register A, while figure 14 presents zero-bit level of Full Adder realized as described in Chapter 2. Figure 15 presents result that is shown on 7-segment display for the add and increment operation, which is generated for the following values of select control and input signals: $S_1S_0C_{in}$=*011, A=0001* and *B=0001*.

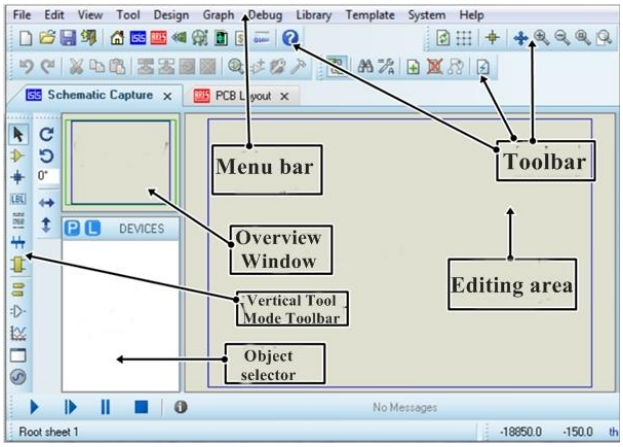

Figure 12. *Starting window of Proteus 8 Demonstration*

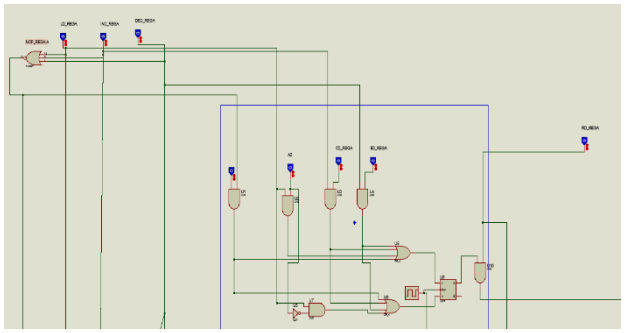

Figure 13. *Zero-bit level of register A realized in Proteus 8 Demonstration*

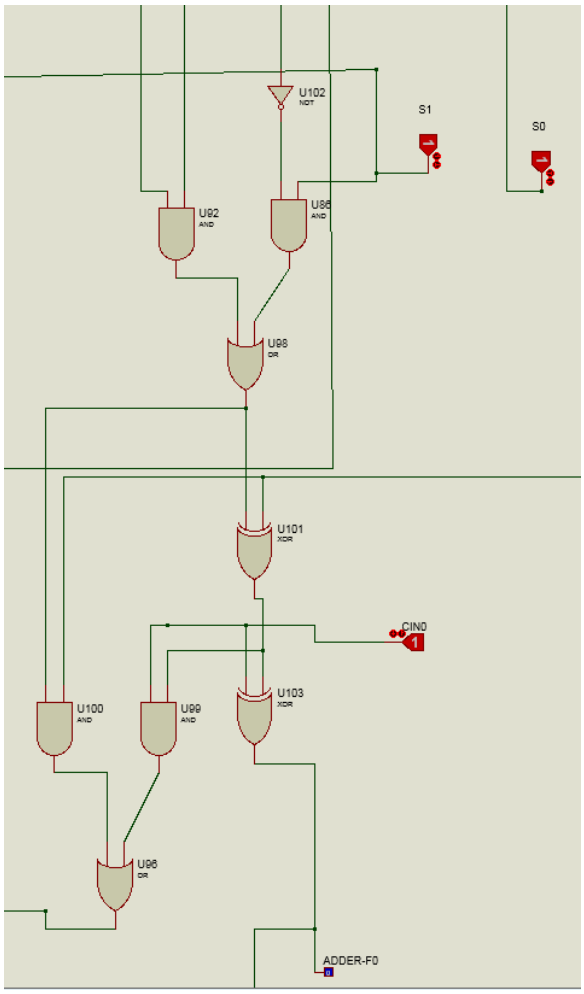

Figure 14. *Zero-bit level of Full Adder realized in Proteus 8 Demonstration*

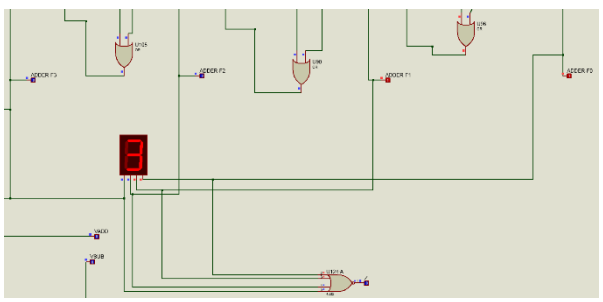

Figure 15. *Result of operation displayed on 7-segment display when* $S_1S_0C_{in}$=011, A=0001 *and* B=0001.

6. RESULTS OF ANALYSIS

This chapter describes list of advantages and disadvantages according certain parameters chosen for analysis of simulators that were described in the chapters before. These parameters are:

1. License required to use a tool;
2. The tool has all (or almost all) modules realized as one whole module;
3. Possibility of tracking input and output signals;
4. Possibility of reducing complexity of the designed scheme;
5. Documentation;
6. Additional tutorials and manuals;
7. Error detection mechanism;
8. Usage of a tool can be described as: the most simple, simple or medium easy.

Advantages of Cedar Logic Simulator:

1. It is free. That means that it does not need the license for using;
2. It has the possibility of tracking input and output signals;
3. It has the possibility of splitting schema – Which reduce complexity in designing schema;
4. It has documentation that describes basic terms for using of this tool;
5. Usage of this tool is described as the most simple.

Disadvantages of Cedar Logic Simulator:

1. It does not have all modules realized as one whole module – This simulator does not have realized T and RS flip-flop and also does not have demultiplexer which is very important disadvantage of this simulator;
2. It does not have additional tutorials and manuals;
3. It does not have mechanism for error detection.

Advantages of Deeds DcS- Digital Circuit Simulator:

1. It is free – it does not need the license for using;
2. It has all modules realized as one whole module;
3. It has the possibility of tracking input and output signals;
4. It has the possibility of hierarchical designing by creating block diagrams of the designed digital circuits. In this way it reduces complexity of the designed scheme;

5. Documentation – It has very detail documentation that describes basic terms for using of this tool and also examples;
6. It has additional tutorials and manuals-which is extremely important for users to understand how to use the tool correctly;
7. It has mechanism for error detection;
8. Usage of this tool is described as simple.

Advantages of Proteus 8 Demonstration:

1. This tool can be partly used without license. For using all features and possibilities of the tool, the license is needed;
2. Documentation – It has very detail documentation that describes basic terms for using of this tool;
3. It has additional tutorials and manuals-which is extremely important for users to understand how to use the tool correctly;
4. It has mechanism for error detection;
5. It has possibility of tracking input and output signals.

Disadvantages of Proteus 8 Demonstration:

1. It does not have all modules realized as one whole module;
2. It does not have possibility of splitting schema, Also, it is not possible to build block elements of the designed digital circuits and this lack reduces efficiency in designing of schema;
3. Usage of this tool is described as medium easy.

7. CONCLUSION

Based on the results of individual and comparative analysis of these three software tools (simulators) according chosen parameters, the most efficient tool was Deeds DcS- Digital Circuit Simulator, then Proteus 8 Demonstration and finally the least efficient was Cedar Logic Simulator. The first ranged tool has no disadvantages according chosen parameters. The second ranged tool is not completely free for students because of its great and rich library, mechanism for error detection, additional manuals and tutorials etc. Although it really deserves second place, because it is better than Cedar Logic Simulator. At the other hand it is slightly worse choice than Deeds DcS-Digital Circuit Simulator, because it is not completely free and it cannot build block elements which would help at reducing complexity of designing schemas.

Deeds DcS-Digital Circuit Simulator and Proteus 8 Demonstration are recommended to be used for students at technical colleges whose major field is either Computer or Software engineering or for the users that would like to get familiar with VHDL programming, microcontrollers etc. On the other hand, due of the absence of certain modules and its simplicity, CEDAR Logic Simulator is recommended for students of those faculties where e.g. subjects such as Fundamentals of Computer Science or Digital Electronics were an optional subject or where these teaching units were covered on a smaller scale comparing to the technical faculties.

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